

## CLAIMS

What is claimed is:

1. A method for interfacing with a modulator in a broadband communication system, the method comprising the steps of:
  - receiving a plurality of packet streams, the packet streams containing a plurality of packets, including packets containing reverse channel synchronization messages;
  - buffering each packet from the plurality of packet streams;
  - detecting a packet identifier within each packet;
  - remapping the packet identifier within each packet; and
  - combining the plurality of packet streams into a single stream.
2. The method of claim 1, wherein the step of remapping the packet identifier comprises the steps of:
  - determining a new packet identifier; and
  - replacing the packet identifier with the new packet identifier.
3. The method of claim 2, wherein the packet identifier comprises a PID.
4. The method of claim 3, wherein the step of remapping the packet identifier within each packet further comprises remapping the packet identifier of stuff packets.
5. The method of claim 4, wherein the method further comprises the step of providing the single data stream to a modulator.

1        6.        The method of claim 5, further comprising the step of adjusting the reverse  
2        channel synchronization message to maintain reverse channel synchronization of each  
3        packet.

1  
1        7.        The method of claim 6, wherein the step of providing the single data stream to a  
2        modulator further comprises remapping the new packet identifier back to the original  
3        packet identifier.

1  
1        8.        A method for interfacing with a modulator in a broadband communication system,  
2        the method comprising the steps of:  
3                receiving a plurality of packet streams, the packet streams containing a plurality of  
4                transport packets, including shared reverse channel timing control information; and  
5                adjusting shared reverse channel timing control information in the plurality of  
6                packets.

1  
1        9.        The method of claim 8, further comprising the steps of integrating the plurality of  
2        packet streams into one stream containing the plurality of transport packets; and  
3                providing the plurality of transport packets to a modulator.

1  
1        10.       The method of claim 9, wherein the step of providing the plurality of transport  
2        packets to a modulator comprises carrying the plurality of transport packets via an  
3        asynchronous serial interface.

1 11. The method of claim 10, wherein the step of providing the plurality of transport  
2 packets to a modulator further comprises carrying the plurality of transport packets on a  
3 plurality of parallel asynchronous serial interfaces.

1 12. The method of claim 11, wherein the modulator comprises a QAM modulator.

1 13. The method of claim 12, wherein the modulator further comprises a multi-QAM  
2 modulator.

1 14. The method of claim 13, wherein the plurality of packet streams containing a  
2 plurality of transport packets further comprises packet streams conforming to the  
3 DOCSIS standard, wherein the plurality of transport packets conforms to the MPEG  
4 protocol, each of the plurality of transport packets having a packet identification.

1 15. The method of claim 14, wherein the step of integrating the plurality of packet  
2 streams into one stream further comprises buffering each of the plurality of packet  
3 streams.

1 16. The method of claim 15, wherein the buffering is performed by a first in first out  
2 buffer.

1  
1 17. The method of claim 16, wherein the step of buffering each of the plurality of  
2 packet streams further comprises the steps of:

3 identifying a packet identifier within the transport packet;

4 determining a new packet identifier; and

5 replacing the packet identifier of the transport packet with the new packet  
6 identifier.

1  
1 18. The method of claim 17, wherein the step of receiving a plurality of packet  
2 streams further comprises receiving at least two separate packet streams wherein the  
3 plurality of transport packets include a reverse channel synchronization message.

1  
1 19. The method of claim 18, wherein the step of adjusting shared reverse channel  
2 timing control information comprises the steps of:

3 parsing the transport packet;

4 detecting a time reference value in the transport packet;

5 determining a location in the transport packet of the time reference value;

6 generating a new time reference value from a clock synchronized with a  
7 system clock; and

8 replacing the detected time reference value in the transport packet  
9 with the new time reference value.

1  
1 20. The method of claim 19, wherein the step of generating a new time reference  
2 value from a clock synchronized with a system clock further comprises the step of  
3 adjusting the new time reference value based on the location in the location in the  
4 transport packet of the time reference value.

1  
1 21. The method of claim 20, wherein the plurality of packet streams containing a  
2 plurality of transport packets further comprises MPEG packet streams conforming to the  
3 MPEG protocol, each MPEG packet stream containing a plurality of MPEG transport  
4 packets, the plurality of MPEG transport packets containing MPEG programming.

1  
1 22. The method of claim 21, further including the step of adjusting an MPEG  
2 transport packet timing, including the step of detecting an adaptation field in an MPEG  
3 transport packet.

1  
2 23. The method of claim 22, wherein the step of adjusting an MPEG transport packet  
3 timing, further comprising the steps of:  
4 detecting the value of timing message within a transportation packet;  
5 generating a replacement timing message; and  
6 replacing the timing message in the transportation packet with the replacement  
7 timing message.

1  
1 24. The method of claim 23, wherein the plurality of packet streams are configured in  
2 parallel with each other.

1  
1 25. The method of claim 24, wherein the plurality of packet streams are configured in  
2 a series.

1  
1 26. The method of claim 25, wherein the plurality of packet streams are configured as  
2 multiple sets of packet streams, each set of packet streams comprising one or more packet  
3 stream configured in a series, each set of packet streams being configured in parallel with  
4 the other sets of packet streams.

1  
1 27. The method of claim 26, wherein the modulator operates at constant latency.

1  
1 28. The method of claim 27, wherein the modulator operates at variable latency.

1  
1 29. The method of claim 28, wherein the method further comprises the step of making  
2 a second adjustment in the plurality of packets to the timing control of the shared reverse  
3 channel.  
1

1  
1 30. An apparatus for interfacing a plurality of information streams, the information  
2 streams comprising data streams conforming to the DOCSIS standard, each data stream  
3 comprising a plurality of transport packets, the plurality of transport packets conforming  
4 to the MPEG protocol, each of the plurality of transport packets having a packet  
5 identification, the apparatus comprising:

6 a plurality of buffers, each buffer containing one of the plurality of information  
7 streams; a selector, configured to select a transport packet from the plurality of buffers;

8 a remapper, configured to remap a packet identification of the transport packet of  
9 the selected stream with a unique packet identification, the unique packet identification  
10 corresponding a source of the information stream; and

11 a time reference adjuster, configured to adjust the time reference of the transport  
12 packet of the selected data stream; and an asynchronous serial interface.

1 31. The apparatus of claim 30, wherein the plurality of information streams further  
2 comprise one or more MPEG streams, each MPEG stream conforming to the MPEG  
3 protocol, each MPEG stream containing a plurality of transport packets, the transport  
4 packets containing MPEG programming.

1 32. The apparatus of claim 31, wherein the selector comprises a state machine.

1 33. The apparatus of claim 32, wherein the apparatus further comprises a QAM  
2 modulator, the QAM modulator configured to receive an input from the asynchronous  
3 serial interface.

1 34. The apparatus of claim 33, wherein the QAM modulator comprises a multi-QAM  
2 modulator.

1 35. The apparatus of claim 34, wherein the asynchronous serial interface comprises  
2 multiple parallel asynchronous serial interfaces.

1 36. The apparatus of claim 35, wherein the plurality of information streams are  
2 configured in parallel with each other.

1 37. The apparatus of claim 36, wherein the plurality of information streams are  
2 configured in a series.

1 38. The apparatus of claim 37, wherein the plurality of information streams are  
2 configured as multiple sets of information streams, each set of information streams  
3 comprising one or more information stream configured in a series, each set of information  
4 streams being configured in parallel with the other sets of information streams.

1 39. An apparatus for interfacing with a modulator in a broadband communication  
2 system, the apparatus comprising:  
3 a plurality of buffers configured to receive individual packets from a plurality of  
4 packet streams including packets containing reverse channel synchronization messages;  
5 a detector configured to detect a packet identifier within each packet;  
6 a remapper configured to remap the packet identifier within each packet; and  
7 an asynchronous serial interface.



1        40.    An apparatus for interfacing with a modulator in a broadband communication  
2        system, the apparatus comprising:

3                a multiplexer configured to integrate a plurality of packet streams into one stream  
4        containing a plurality of transport packets, including packets sharing a reverse channel;  
5        and

6                a timing control adjuster configured to adjust the timing control of the shared  
7        reverse channel in the plurality of packets.

1        41.    The apparatus of claim 40, further comprising:

2                a remapper configured to remap a packet identifier within each packet; and  
3                an asynchronous serial interface connected to the timing control adjuster.